

MC74LVXT4051

Analog Multiplexer/ Demultiplexer High-Performance Silicon-Gate CMOS

The MC74LVXT4051 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The LVXT4051 is similar in pinout to the LVX8051, the HC4051A, and the metal-gate MC14051B. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard TTL levels. These inputs are over-voltage tolerant (OVT) for level translation from 6.0 V down to 3.0 V.

This device has been designed so the ON resistance (R_{ON}) is more linear over input voltage than the R_{ON} of metal-gate CMOS analog switches and High-Speed CMOS analog switches.

Features

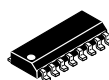
- Select Pins Compatible with TTL Levels
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Analog Power Supply Range ($V_{CC} - V_{EE}$) = -3.0 V to +3.0 V
- Digital (Control) Power Supply Range ($V_{CC} - GND$) = 2.5 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal-Gate, HSL, or VHC Counterparts
- Low Noise
- Designed to Operate on a Single Supply with $V_{EE} = GND$, or Using Split Supplies up to ± 3.0 V
- Break-Before-Make Circuitry
- Pb-Free Packages are Available*



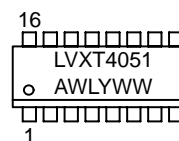
ON Semiconductor®

<http://onsemi.com>

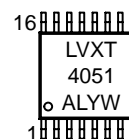
MARKING DIAGRAMS



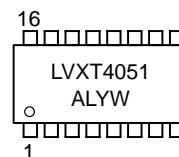
SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



SOEIAJ-16
M SUFFIX
CASE 966



A = Assembly Location
WL or L = Wafer Lot
Y = Year
WW or W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74LVXT4051

FUNCTION TABLE

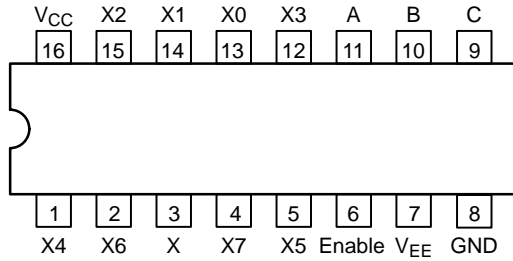


Figure 1. Pin Connection and Marking Diagram
(Top View)

Control Inputs				ON Channels
Enable	Select			
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

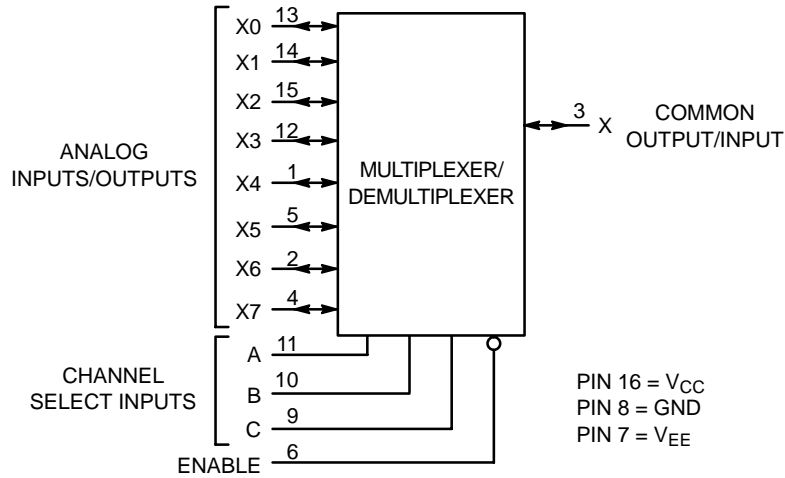


Figure 2. Logic Diagram
Single-Pole, 8-Position Plus Common Off

ORDERING INFORMATION

Device	Package	Shipping†
MC74LVXT4051D	SOIC-16	48 Units / Rail
MC74LVXT4051DG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74LVXT4051DR2	SOIC-16	2500 Tape & Reel
MC74LVXT4051DR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LVXT4051DT	TSSOP-16*	96 Units / Rail
MC74LVXT4051DTR2	TSSOP-16*	2500 Tape & Reel
MC74LVXT4051M	SOEIAJ-16	50 Units / Rail
MC74LVXT4051MG	SOEIAJ-16 (Pb-Free)	50 Units / Rail
MC74LVXT4051MEL	SOEIAJ-16	2000 Tape & Reel
MC74LVXT4051MELG	SOEIAJ-16 (Pb-Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MC74LVXT4051

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	- 7.0 to + 0.5	V
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	- 0.5 to + 7.0 - 0.5 to + 7.0	V
V_{IS}	Analog Input Voltage	$V_{EE} - 0.5$ to $V_{CC} + 0.5$	V
V_{IN}	Digital Input Voltage (Referenced to GND)	- 0.5 to 7.0	V
I	DC Current, Into or Out of Any Pin	± 20	mA
T_{STG}	Storage Temperature Range	- 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature under Bias	+ 150	°C
θ_{JA}	Thermal Resistance	SOIC 143 TSSOP 164	°C/W
P_D	Power Dissipation in Still Air,	SOIC 500 TSSOP 450	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating	Oxygen Index: 30% – 35% UL 94-V0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) > 2000 Machine Model (Note 2) > 200 Charged Device Model (Note 3) > 1000	V
$I_{LATCHUP}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 4)	± 300 mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	- 6.0	GND	V
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	2.5 2.5	6.0 6.0	V
V_{IS}	Analog Input Voltage	V_{EE}	V_{CC}	V
V_{IN}	Digital Input Voltage (Note 5) (Referenced to GND)	0	6.0	V
T_A	Operating Temperature Range, All Package Types	- 55	125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs)	$V_{CC} = 3.0 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$	0 100 20	ns/V

5. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

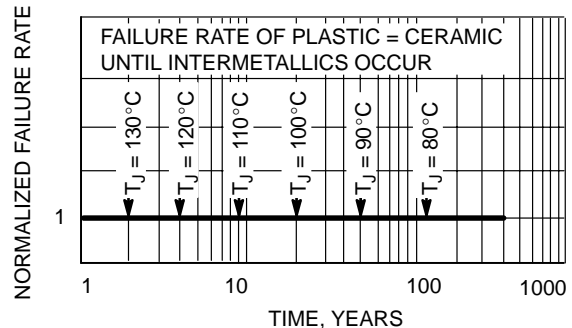


Figure 3. Failure Rate vs. Time Junction Temperature

MC74LVXT4051

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs		3.0	2.0	2.0	2.0	V
			4.5	2.0	2.0	2.0	
			5.5	2.0	2.0	2.0	
V _{IL}	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs		3.0	0.5	0.5	0.5	V
			4.5	0.8	0.8	0.8	
			5.5	0.8	0.8	0.8	
I _{IN}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V _{IN} = 6.0 or GND	0 V to 6.0 V	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V _{IS} = V _{CC} or GND	6.0	4.0	40	80	μA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Test Conditions	V _{CC} V	V _{EE} V	Guaranteed Limit			Unit
					–55 to 25°C	≤85°C	≤125°C	
R _{ON}	Maximum “ON” Resistance	V _{IN} = V _{IL} or V _{IH} V _{IS} = 1/2 (V _{CC} – V _{EE}) I _S = 2.0 mA (Figure 4)	3.0	0	86	108	120	Ω
			4.5	0	37	46	55	
			3.0	–3.0	26	33	37	
ΔR _{ON}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V _{IN} = V _{IL} or V _{IH} V _{IS} = 1/2 (V _{CC} – V _{EE}) I _S = 2.0 mA	3.0	0	15	20	20	Ω
			4.5	0	13	18	18	
			3.0	–3.0	10	15	15	
I _{off}	Maximum Off-Channel Leakage Current, Any One Channel	V _{in} = V _{IL} or V _{IH} ; V _{IO} = V _{CC} or GND; Switch Off (Figure 3)	5.5 +3.0	0 –3.0	0.1 0.1	0.5 0.5	1.0 1.0	μA
	Maximum Off-Channel Leakage Current, Common Channel	V _{in} = V _{IL} or V _{IH} ; V _{IO} = V _{CC} or GND; Switch Off (Figure 4)	5.5 +3.0	0 –3.0	0.2 0.2	2.0 2.0	4.0 4.0	
I _{on}	Maximum On-Channel Leakage Current, Channel-to-Channel	V _{in} = V _{IL} or V _{IH} ; Switch-to-Switch = V _{CC} or GND; (Figure 5)	5.5 +3.0	0 –3.0	0.2 0.2	2.0 2.0	4.0 4.0	μA

AC CHARACTERISTICS (Input t_r = t_f = 3 ns)

Symbol	Parameter	Test Conditions	V _{CC} V	V _{EE} V	Guaranteed Limit				Unit
					–55 to 25°C		≤85°C	≤125°C	
					Min	Typ*			
t _{BBM}	Minimum Break-Before-Make Time	V _{IN} = V _{IL} or V _{IH} V _{IS} = V _{CC} R _L = 300 Ω, C _L = 35 pF (Figures 12 and 13)	3.0	0.0	1.0	6.5	–	–	ns
			4.5	0.0	1.0	5.0	–	–	
			3.0	–3.0	1.0	3.5	–	–	

*Typical Characteristics are at 25°C.

MC74LVXT4051

AC CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 3$ ns)

Symbol	Parameter	V_{CC} V	V_{EE} V	Guaranteed Limit						Unit	
				- 55 to 25°C			≤ 85°C		≤ 125°C		
				Min	Typ	Max	Min	Max	Min		Max
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figures 16 and 17)	2.5	0			40		45		50	ns
		3.0	0			28		30		35	
		4.5	0			23		25		30	
		3.0	-3.0			23		25		28	
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figures 14 and 15)	2.5	0			40		45		50	ns
		3.0	0			28		30		35	
		4.5	0			23		25		30	
		3.0	-3.0			23		25		28	
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figures 14 and 15)	2.5	0			40		45		50	ns
		3.0	0			28		30		35	
		4.5	0			23		25		30	
		3.0	-3.0			23		25		28	

		Typical @ 25°C, $V_{CC} = 5.0$ V, $V_{EE} = 0$ V			
C_{PD}	Power Dissipation Capacitance (Figure 18) (Note 6)	45			pF
C_{IN}	Maximum Input Capacitance, Channel–Select or Enable Inputs	10			pF
$C_{I/O}$	Maximum Capacitance (All Switches Off)	Analog I/O	10		pF
		Common O/I	10		
		Feedthrough	1.0		

6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	V_{EE} V	Typ	Unit
					25°C	
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response	$V_{IS} = \frac{1}{2} (V_{CC} - V_{EE})$ Ref and Test Attn = 10 dB Source Amplitude = 0 dB (Figure 7)	3.0	0.0	80	MHz
			4.5	0.0	80	
			6.0	0.0	80	
			3.0	-3.0	80	
V_{ISO}	Off–Channel Feedthrough Isolation	$f = 1$ MHz; $V_{IS} = \frac{1}{2} (V_{CC} - V_{EE})$ Adjust Network Analyzer output to 10 dBm on each output from the power splitter. (Figures 8 and 9)	3.0	0.0	-70	dB
			4.5	0.0	-70	
			6.0	0.0	-70	
			3.0	-3.0	-70	
V_{ONL}	Maximum Feedthrough On Loss	$V_{IS} = \frac{1}{2} (V_{CC} - V_{EE})$ Adjust Network Analyzer output to 10 dBm on each output from the power splitter. (Figure 11)	3.0	0.0	-2	dB
			4.5	0.0	-2	
			6.0	0.0	-2	
			3.0	-3.0	-2	
Q	Charge Injection	$V_{IN} = V_{CC}$ to V_{EE} , $f_{IS} = 1$ kHz, $t_r = t_f = 3$ ns $R_{IS} = 0 \Omega$, $C_L = 1000$ pF, $Q = C_L * \Delta V_{OUT}$ (Figure 10)	5.0	0.0	9.0	pC
			3.0	-3.0	12	
THD	Total Harmonic Distortion THD + Noise	$f_{IS} = 1$ MHz, $R_L = 10$ K Ω , $C_L = 50$ pF, $V_{IS} = 5.0$ V $_{PP}$ sine wave $V_{IS} = 6.0$ V $_{PP}$ sine wave (Figure 19)	6.0	0.0	0.10	%
			3.0	-3.0	0.05	

MC74LVXT4051

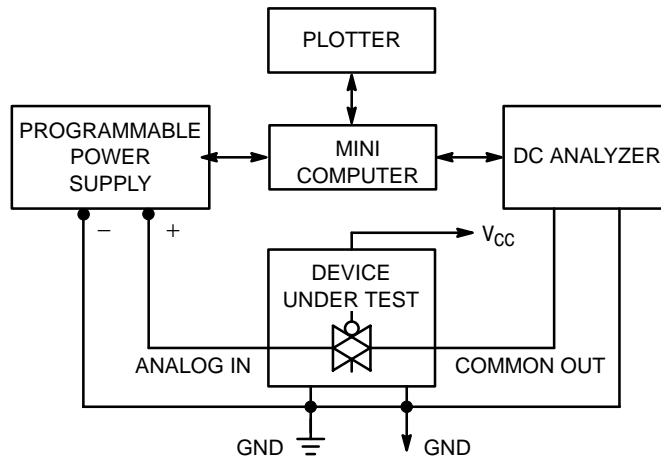


Figure 4. On Resistance, Test Set-Up

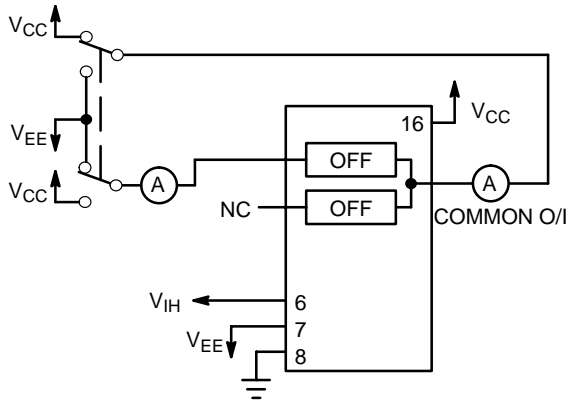


Figure 5. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

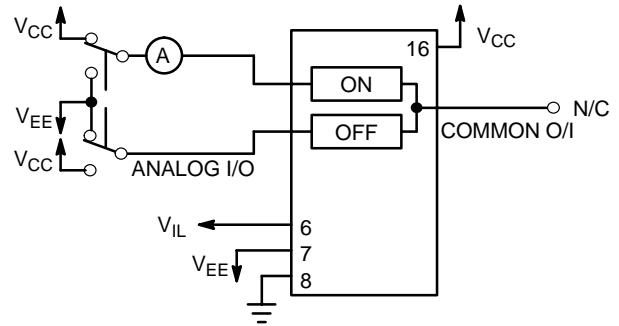


Figure 6. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up

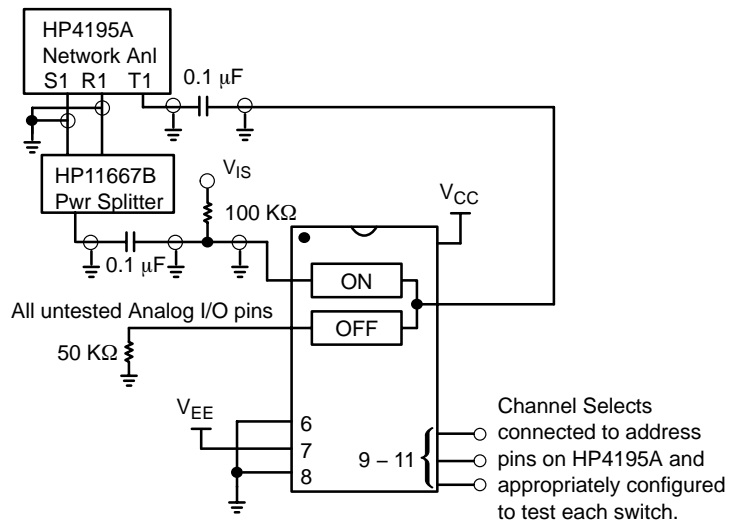
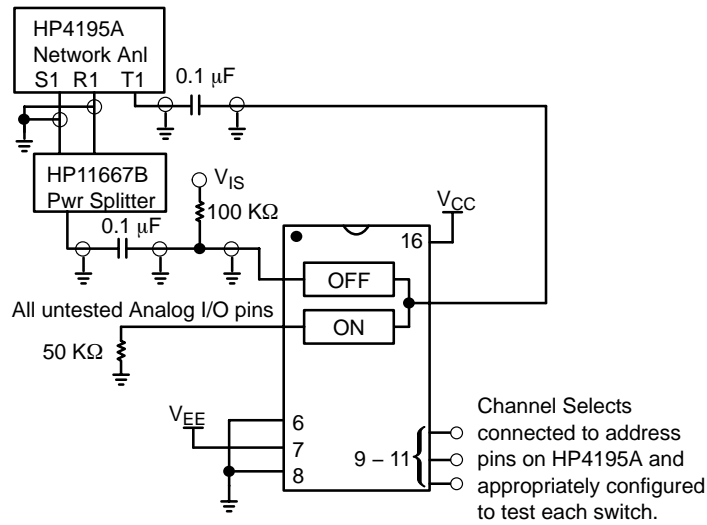


Figure 7. Maximum On Channel Bandwidth, Test Set-Up

MC74LVXT4051



Config = Network
 Format = T/R (dB)
 CAL = Trans Cal
 Display = Rectan X - A + B $V_{ISO}(dB) = 20 \log (V_{T1}/V_{R1})$
 Scale Ref = Auto Scale
 View = Off, Off, Off
 Trig = Cont Mode
 Source Amplitude = + 13 dB
 Reference Attenuation = 20 dB
 Test Attenuation = 0 dB

Figure 8. Maximum Off Channel Feedthrough Isolation, Test Set-Up

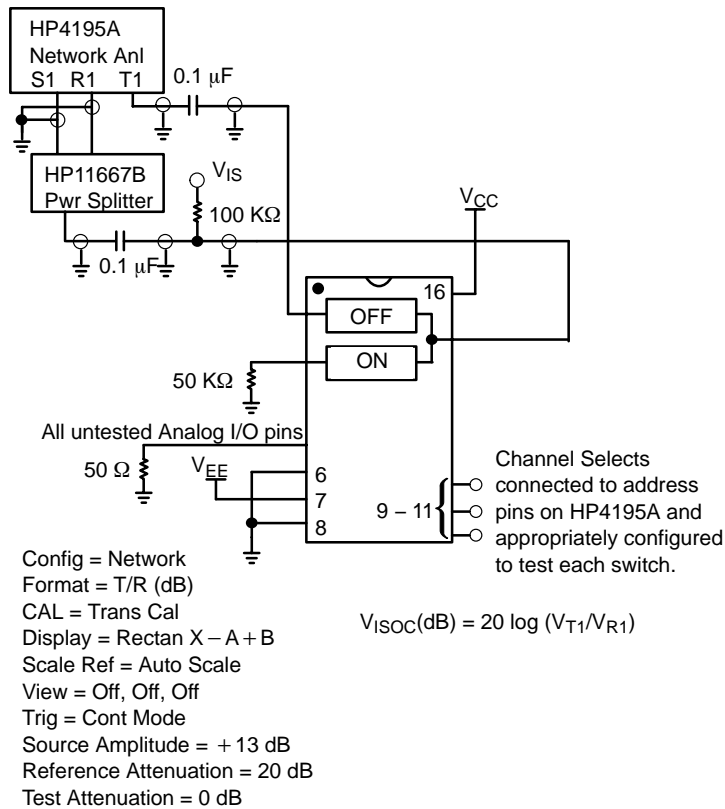
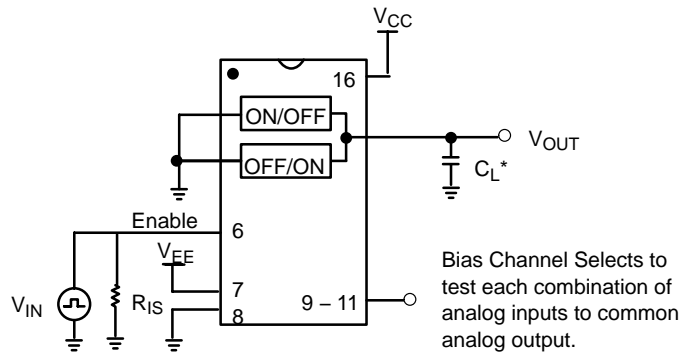


Figure 9. Maximum Common-Channel Feedthrough Isolation, Test Set-Up

MC74LVXT4051



*Includes all probe and jig capacitance.

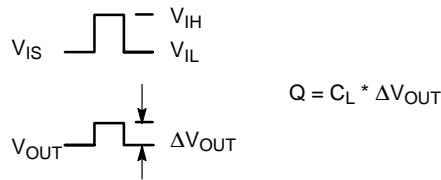


Figure 10. Charge Injection, Test Set-Up

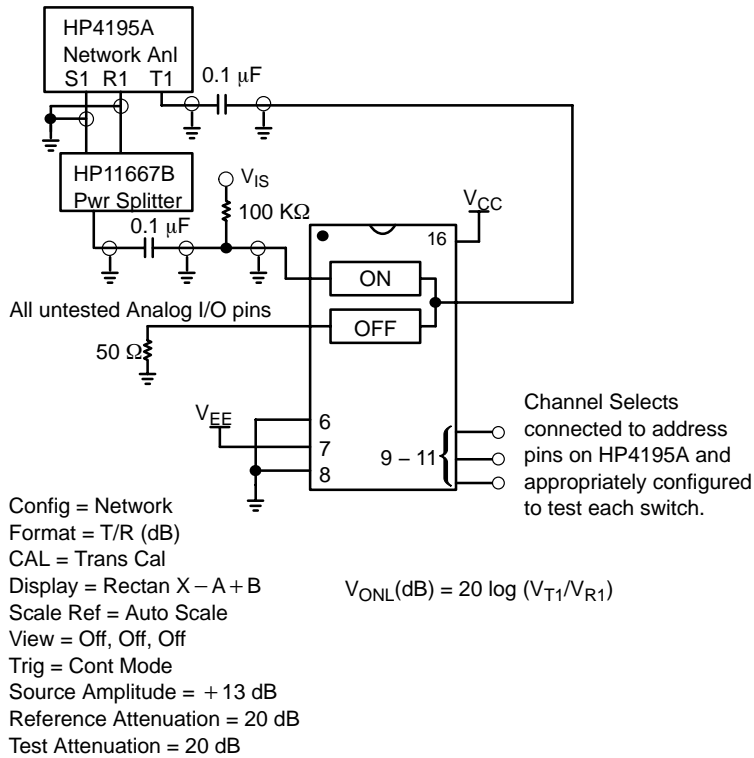


Figure 11. Maximum On Channel Feedthrough On Loss, Test Set-Up

MC74LVXT4051

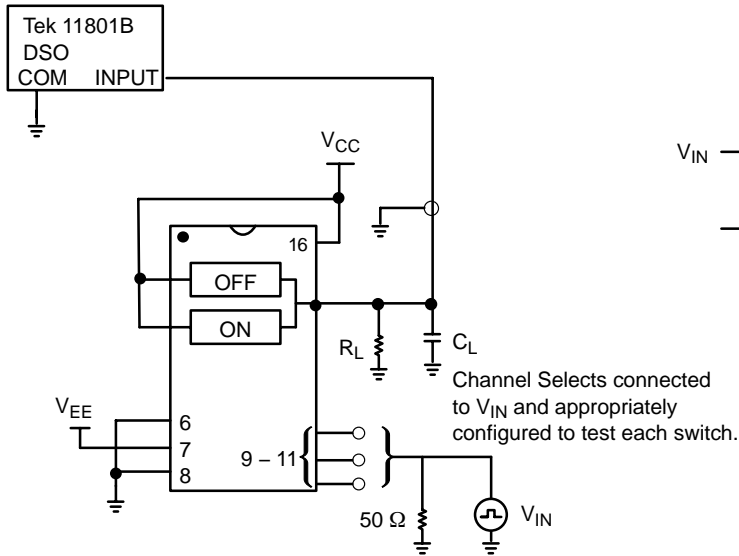


Figure 12. Break-Before-Make, Test Set-Up

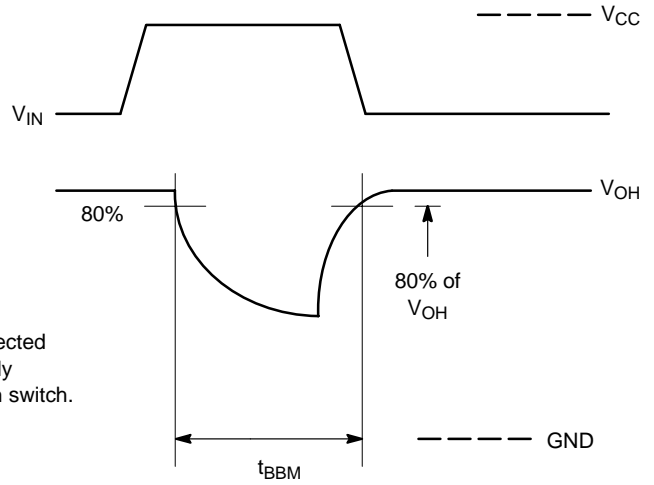


Figure 13. Break-Before-Make Time

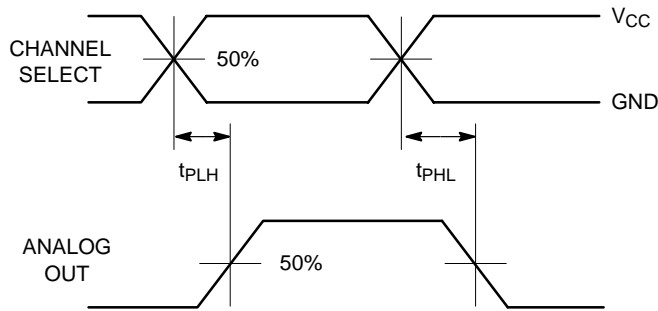
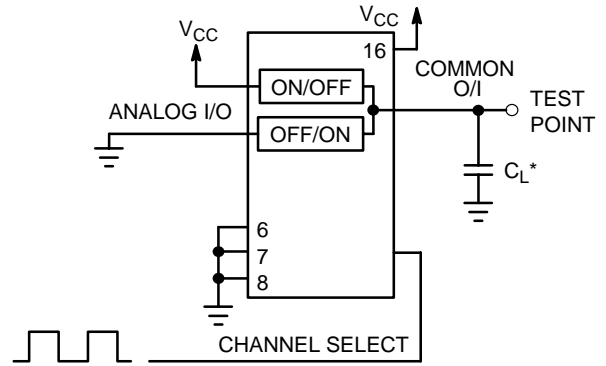


Figure 14. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance.

Figure 15. Propagation Delay, Test Set-Up Channel Select to Analog Out

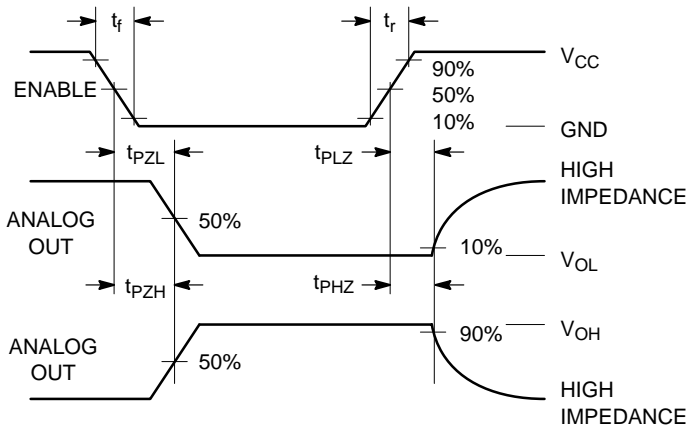


Figure 16. Propagation Delays, Enable to Analog Out

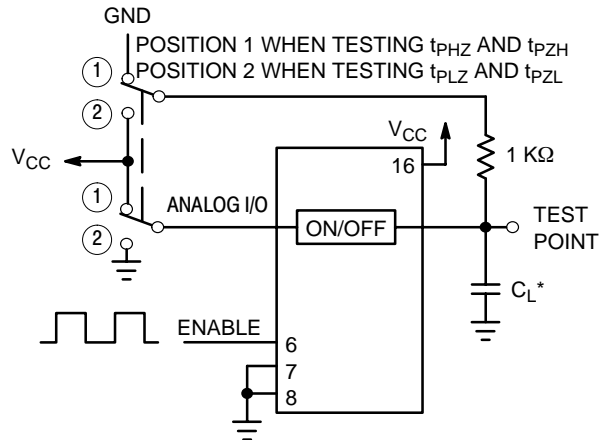


Figure 17. Propagation Delay, Test Set-Up Enable to Analog Out

MC74LVXT4051

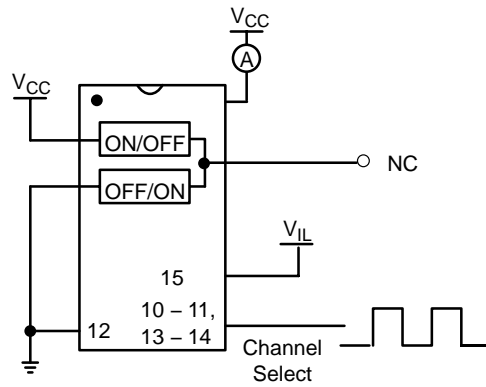


Figure 18. Power Dissipation Capacitance, Test Set-Up

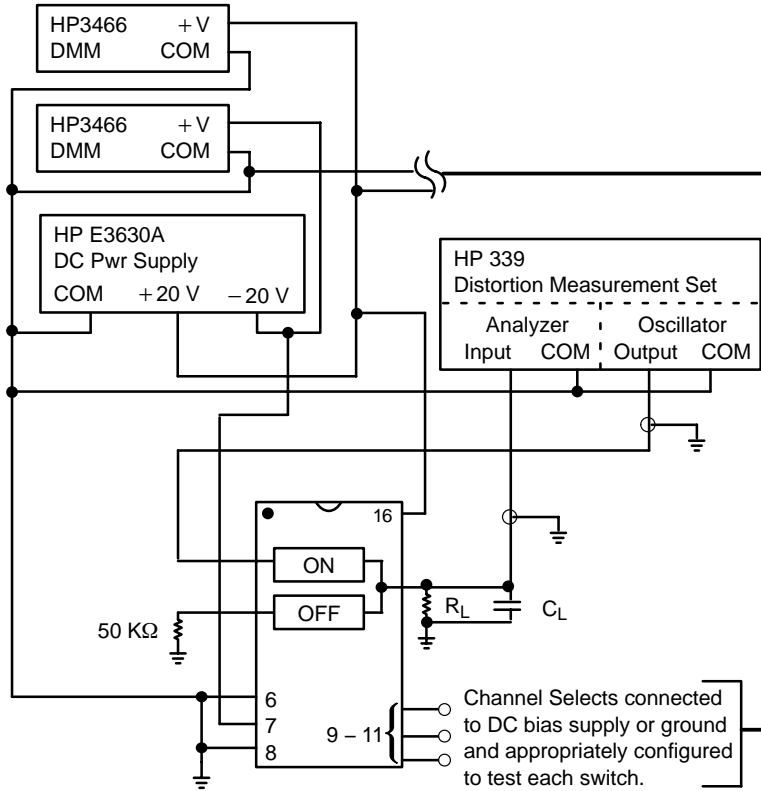


Figure 19. Total Harmonic Distortion, Test Set-Up

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$$V_{CC} = +5 \text{ V} = \text{logic high}$$

$$GND = 0 \text{ V} = \text{logic low}$$

The maximum analog voltage swing is determined by the supply voltages V_{CC} and V_{EE} . The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below V_{EE} . In this example, the difference between V_{CC} and V_{EE} is five volts. Therefore, using the configuration of Figure 21, a maximum analog signal of five volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and

outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$V_{EE} - GND = 0 \text{ to } -6 \text{ volts}$$

$$V_{CC} - GND = 2.5 \text{ to } 6 \text{ volts}$$

$$V_{CC} - V_{EE} = 2.5 \text{ to } 6 \text{ volts}$$

$$\text{and } V_{EE} \leq GND$$

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_x) are recommended as shown in Figure 22. These diodes should be able to absorb the maximum anticipated current surges during clipping.

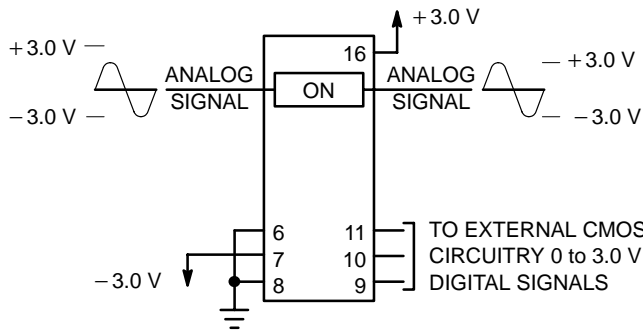


Figure 20. Application Example

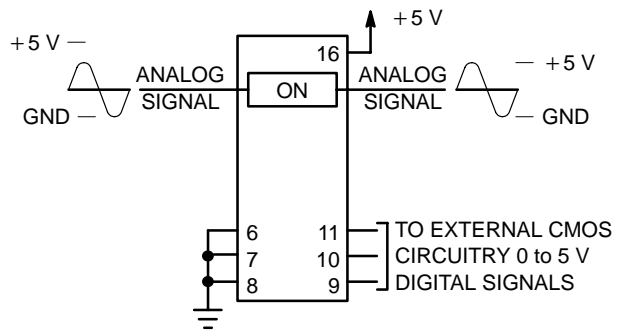


Figure 21. Application Example

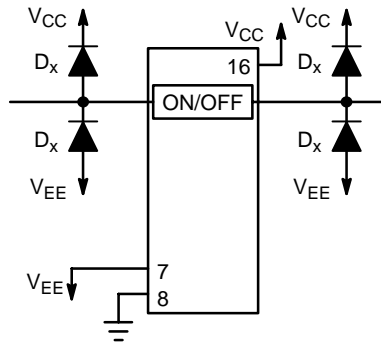


Figure 22. External Germanium or Schottky Clipping Diodes

MC74LVXT4051

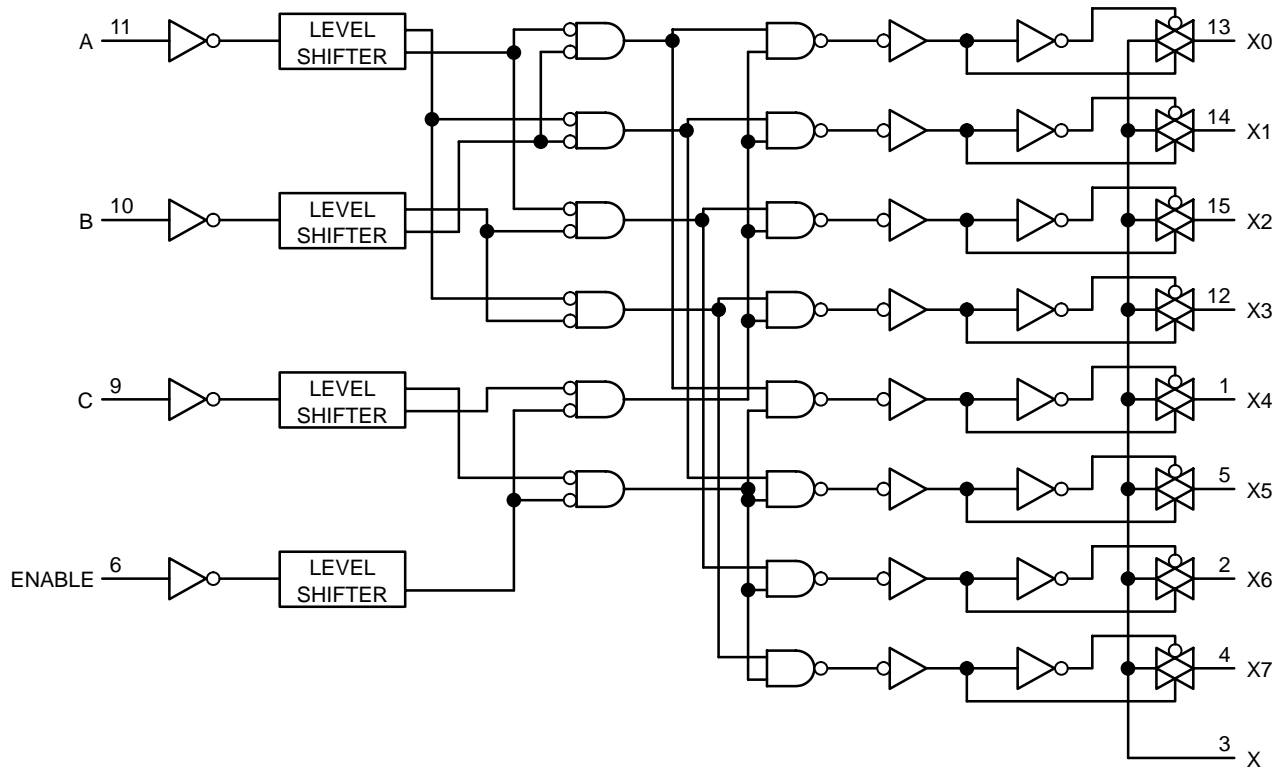
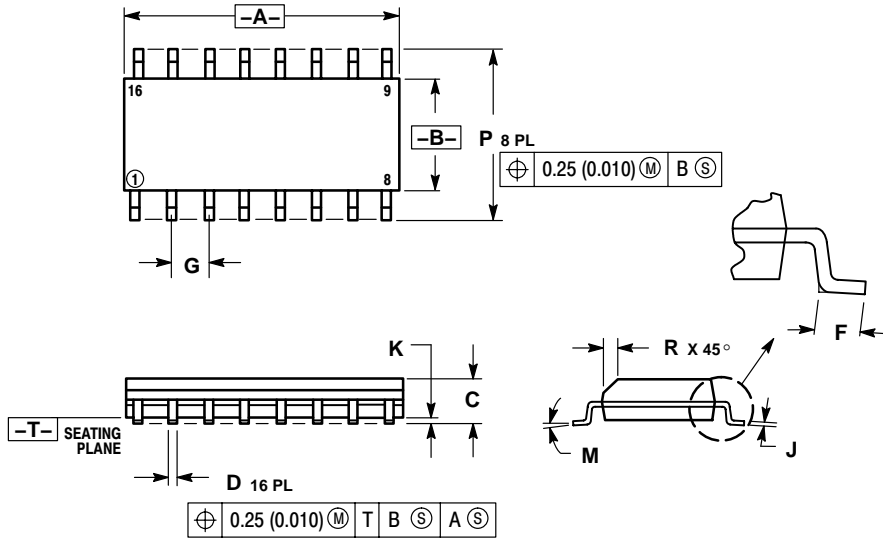


Figure 23. Function Diagram, LVXT4051

MC74LVXT4051

PACKAGE DIMENSIONS

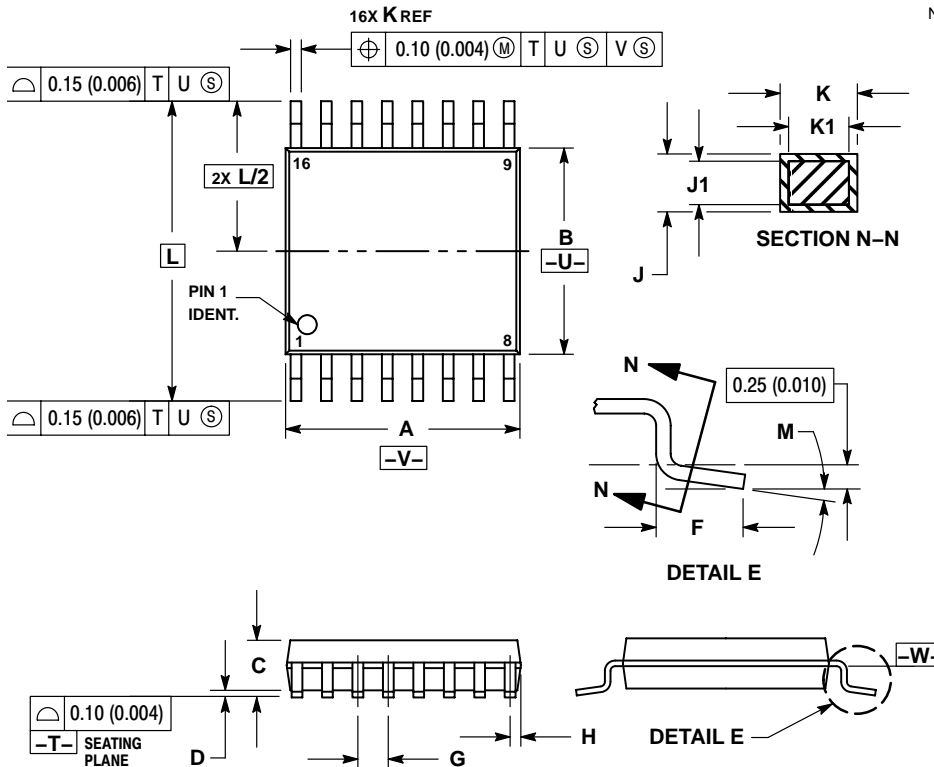
SOIC-16
D SUFFIX
CASE 751B-05
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE A

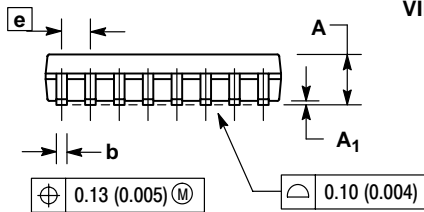
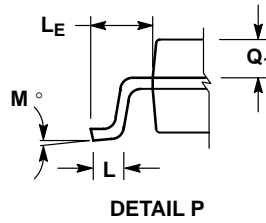
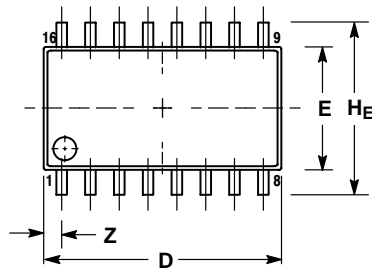


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74LVXT4051


SOEIAJ-16
M SUFFIX
CASE 966-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.